

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A test signal attenuation circuit comprising:
a signal transmitter;
~~a circuit for generating a binary-level waveform;~~
a pulse-shaping circuit for providing a chopping signal ~~for a square~~
5 ~~type waveform;~~ and
a chopping circuit that combines ~~for combining said an original~~
binary-level waveform and said chopping signal to produce an attenuated
chopped signal having less energy content than said original, ~~generated~~ binary-
level waveform, wherein:
10 said attenuated chopped signal is fed to said signal
transmitter; and
said signal transmitter transmits said attenuated chopped
signal at lower signal-to-noise ratio compared to transmission of said original
binary-level waveform.
2. ~~[.]~~ (Currently amended) The attenuation circuit of claim 1 wherein
said chopping circuit provides an attenuated chopped signal having a narrower
pulse width than the original binary-level waveform.
3. (Original) The attenuation circuit of claim 2 wherein said chopping
circuit provides an attenuated chopped signal having the same amplitude as the

original binary-level waveform.

4. (Currently amended) The attenuation circuit of claim 1 ~~[[3]] further~~
including ~~a pulse shaping circuit for forming attenuated pulses in the chopped~~
~~attenuated signal~~ wherein said attenuated chopped signal produces a higher
bit-error rate in a link to said signal transmitter than the original binary-level
5 waveform.

5. (Currently amended) The attenuation circuit of claim 1 ~~[[4]]~~
wherein said pulse shaping circuit converts clock pulses into the ~~attenuated~~
~~chopped~~ chopping signal waveform that is delayed with respect to the bit
intervals of an original binary level waveform.

6-7. (Canceled)

8.~~[[.]]~~ (Currently amended): A test signal attenuation circuit comprising:
a signal transmitter;
~~a circuit for generating a binary-level waveform;~~
a pulse-shaping circuit for providing a chopping signal ~~for a binary-~~
5 ~~level waveform;~~ and
a chopping circuit that combines ~~for combining said an original~~
binary-level waveform and said chopping signal to produce an attenuated
chopped signal having less energy content than said original binary-level
waveform~~[[.]]~~ , wherein:
10 said chopping circuit providing an attenuated chopped
signal having has a narrower pulse width than the original binary-level
waveform;
said attenuated chopped signal is fed to said signal
transmitter; and

15 said signal transmitter transmits said attenuated chopped signal at lower signal-to-noise ratio compared to transmission of said original binary-level waveform.

9.[.] (Currently amended): The test signal attenuation circuit of claim 8 wherein said chopping circuit provides an attenuated chopped signal having the same amplitude as the original binary-level waveform.

10. (Currently amended)The test signal attenuation circuit of claim 8 ~~[[9]] further including a pulse shaping circuit for forming attenuated pulses in the chopped attenuated signal wherein said attenuated chopped signal produces a~~ higher bit-error rate in a link including said signal transmitter.

11. (Currently amended)The test signal attenuation circuit of claim 10 wherein said pulse shaping circuit converts clock pulses into the ~~attenuated chopped~~ chopping signal waveform that is delayed with respect to the bit intervals of an original binary level waveform.

12. (Currently amended): A test signal attenuation circuit comprising:
a signal transmitter;
~~a circuit for generating a binary level waveform;~~
a pulse-shaping circuit for providing a chopping signal from a clock
5 signal for a binary level waveform;
a chopping circuit that combines ~~for combining said an original~~ binary-level waveform and said chopping signal to produce an attenuated chopped signal having less energy content than said original, ~~generated~~ binary-level waveform; and wherein
10 ~~said chopping circuit providing an attenuated chopped signal having~~ has a narrower pulse width than the original binary-level waveform;

said attenuated chopped signal is fed to said signal transmitter; and

- 15 said signal transmitter transmits said attenuated chopped signal at lower signal-to-noise ratio with a higher bit error rate compared to transmission of said original binary-level waveform.

13. (Original) The test signal attenuation circuit of claim 12 wherein said chopping circuit provides an attenuated chopping signal having the same amplitude as the original binary-level waveform.

14. (Currently amended): A method of developing an electrical test signal comprising the steps of:

- ~~activating a signal transmitter;~~
 generating a binary-level waveform;
5 ~~providing a chopping signal for a square-type waveform; and~~
 combining said binary-level waveform and said chopping signal to produce an attenuated chopped signal having less energy content than the original binary-level waveform; and
 transmitting said attenuated chopped signal at a lower signal-to-
10 noise ratio with a higher bit error rate than would occur by transmitting said
binary-level waveform.